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Flash memory is a non-volatile storage device that can be electrically erased and reprogrammed.
Major Markets

[Bar chart showing growth in million GB from 2007 to 2014 across various market categories such as Other, Solid State Drives, Digital Video Camcorders, Personal Navigation Devices, Digital Still Cameras, Mobile Phones, MP3/PMP Players, USB Flash Drives, and Flash Memory Cards.]

Jiroft Inscription - 2600 BCE
EPROM, Dov Frohman, Intel - 1971

Flash Memory
First F-N Tunneling Floating gate EEPROM

**ELECTRICALLY ERASABLE NON-VOLATILE SEMICONDUCTOR MEMORY**

Inventor: Eliyahou Harari, Irvine, Calif.
Assignee: Hughes Aircraft Company, Culver City, Calif.
Appl. No.: 770,346
Filed: Feb. 22, 1977

Related U.S. Application Data

A predetermined section of this insulating layer is relatively thin to permit this section of the floating gate to be relatively close to a corresponding predetermined section of the transistor, thus facilitating the transfer of charges between the transistor substrate and the gate.

Erasing is achieved by removing the charges from the floating gate by reverse tunneling through the relatively thinner insulator region.
United States Patent
Masuoka et al.

[54] SEMICONDUCTOR MEMORY DEVICE AND METHOD FOR MANUFACTURING THE SAME

[75] Inventors: Fujio Masuoka; Hisakazu Izuka, both of Yokohama, Japan

[73] Assignee: Tokyo Shibaura Denki Kabushiki Kaisha, Kawasaki, Japan

[21] Appl. No.: 320,936
[22] Filed: Nov. 13, 1981

[30] Foreign Application Priority Data

[51] Int. Cl.3 ........................................ G11C 11/40
[52] U.S. Cl. .......................................... 365/218; 365/185
[58] Field of Search .................................. 365/185, 218

[56] References Cited
U.S. PATENT DOCUMENTS
4,203,158 5/1980 Frohman-Benschkowsky et al. ............................. 365/185

OTHER PUBLICATIONS
Kupec et al., Triple Level Poly-Silicon E²Prom with Single Transistor Per Bit, 1980, IEEE.

Primary Examiner—Terrell W. Fears
Attorney, Agent, or Firm—Finnegan, Henderson, Farabow, Garrett & Dunner

[57] ABSTRACT
An erase gate is formed for erasing data from a floating gate in a semiconductor memory device having the floating gate and a control gate.
Furthermore, in order to achieve electrical insulation between the erase gate and the control gate, an insulating film formed between the erase gate and the control gate is made thicker than an insulating film formed between the floating gate and the erase gate.

4 Claims, 58 Drawing Figures
SanDisk’s System-Flash Solution (1988)

Goals: Data Store, ~1M W/E, Low cost

Radical new Flash-chip architecture:
- Emulate HDD (Sector/header)
- Parallel page write, multi sector erase, serial read
- Stepped Vpg/Ver, bit by bit inhibit, prog. ref. cells
- MLC

Close-Loop Intelligent Hardware Controller:
- Manage HDD files
- Host Independent, Standard mass storage I/O
- Dynamically manage defective bits/sectors (ECC, retry, recovery, substitution, links)
- Wear-out leveling, hot count
- Adaptive W/E voltages
- Random, direct access interface.
- Fast random reads.
- Slow erase/writes.
NAND Flash

- Higher density, lower cost.
- Fast erase/write.
- Block input/output access.
Single, Multi, and 3-bit Level Flash Cells

SLC
One bit per cell

MLC
Two bits per cell
Block Level Access

- Minimal working unit, depends on size/technology.
- No read/write operation simultaneously.
- Erasing a block sets all bits to 1.
- Programming changes bits from 1 to 0.
Data Retention

Finite number of P/E cycles.
- Wear leveling.
- Bad block management.
Write Amplification

\[
\text{write amplification factor} = \frac{\text{data that controller has to write}}{\text{data that host wants to write}}
\]
Write and Read Disturb

- Write Data Here
- Disturb Data Here
- Read Data Here
- Disturb Data Here

Erase Block

Write Page
Summary

- block-level access
- wear leveling
- read disturb
- bad blocks management
- garbage collection
- different physics
- different interfaces
Sources

- http://persianwondersvideo.blogspot.co.il/2007/02/jiroft.html

Leon Romanovsky  leon@leon.nu  Flash Memory